AMPSS™
Astec Modular Power Supply System

APA100 Power Factor Correction Series

750 - 1200W Output Power
AC-DC Converter Module
Technical Reference Manual

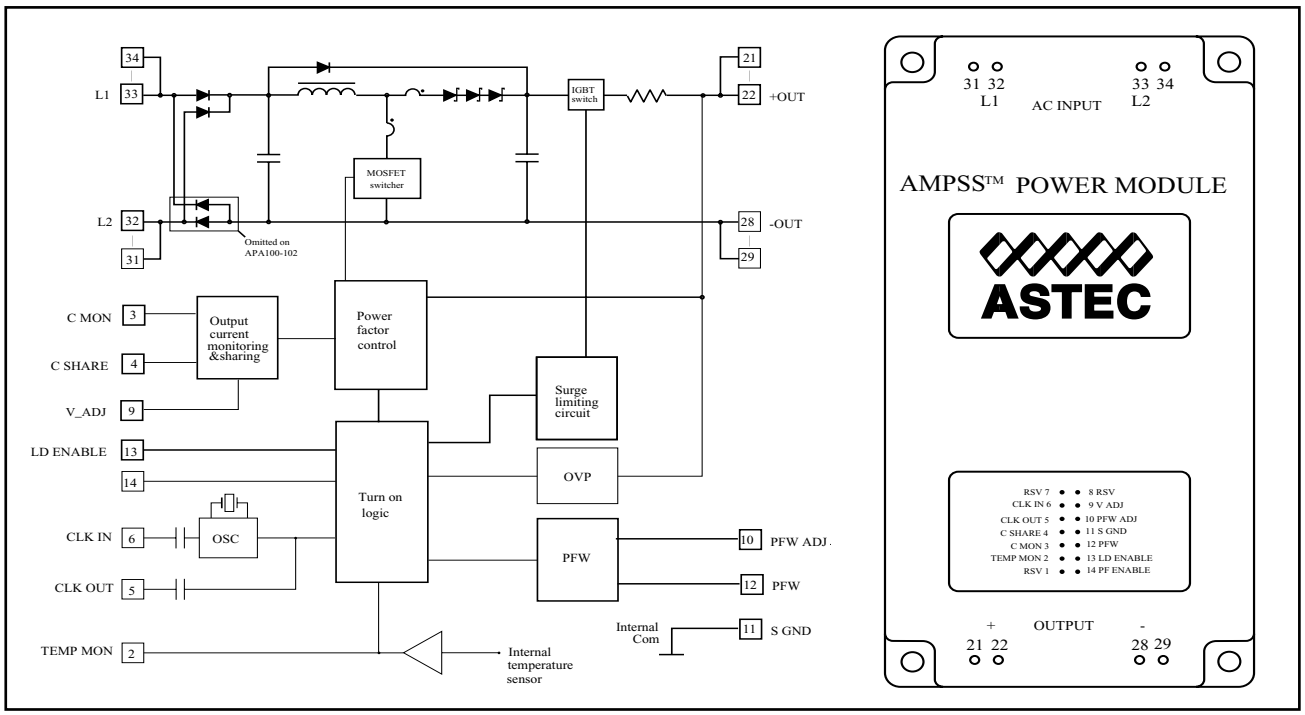
Series Highlights

- Unity Power Factor - 0.99
- High efficiency - up to 95%
- Universal input voltage and frequency
- High Reliability - over 1 million hours MTBF
- Up to 1200W output power

Contents

APA100 Power Factor Correction Series AC-DC Converters

APA100-101/102



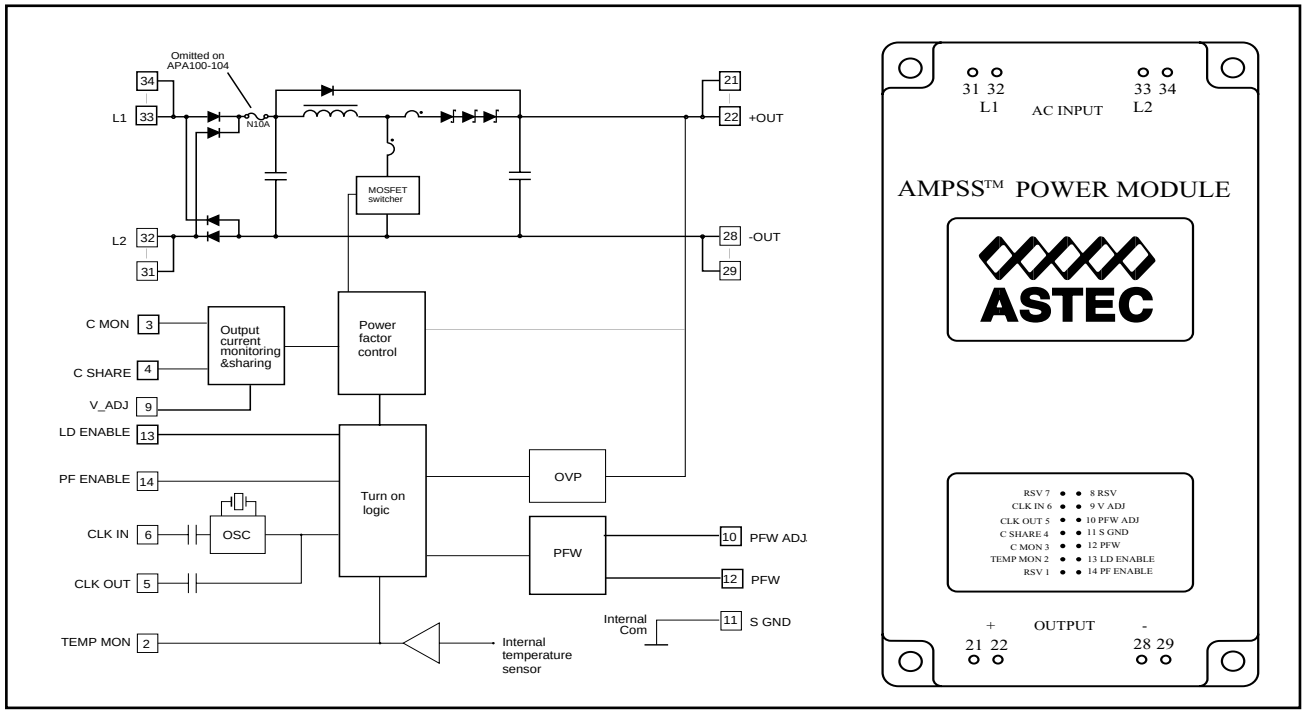
Introduction

The PFC Power Factor Correction module is part of Astecs family of advanced High Density modular power supply components. Featuring high reliability and convenient control and monitoring functions, these modules are designed to reduce product development time and enhance system performance. The PFC is designed to work over all typical line voltages used worldwide, and provide unity power factor with very low levels of harmonic distortion in line current. The PFC includes active start-up current control and short circuit protection circuitry. Power Line Disturbance (PLD) circuitry copes with a wide range of input voltage fluctuations.

Special Features

- Unity Power Factor
- High Efficiency - up to 95%
- Universal input voltage and frequency range
- Up to 1200W output power
- Parallelable with current sharing within 3%
- < 10% harmonic distortion conforming to IEC 1000-3-2
- 85°C baseplate/ Case operating temperature.
- High Reliability - over 1 million hours MTBF
- Programmable Power Fail Warning Signal
- Enable output to control AMPSS™ DC-DC converters

APA100-103/104



The APA100-103/104 is a modified version of the APA100-101 module.

The module differs from the APA100-101/102 in the following respects:

a) IGBT and Surge Limiting Circuitry have been removed (see schematic above).

b) Need an external inrush limiting circuit.

c) The PFW function has been enhanced to cover fault conditions (OTP, OVP, general module fault) and disable.

d) The function of the PF Enable has changed. With the PF Enabled the output is power factor corrected and boosted. With PF Disabled the output is the AC input voltage rectified.

e) Short Circuit Protection during start-up has been removed.

f) The Soft Start-up function has been removed.

g) There is a 10A fuse at the input of APA100-103. Other PFC modules do not have the fuse.

Ordering Information

Model Number	Input Voltage	Output Voltage	Output Power	Notes
APA100-101*	85-265Vac	385Vdc	1200W	For Parallel operation the total input current must be < 16A rms
APA100-102*	85-265Vac	385Vdc	1200W	For Parallel operation where the total input current is > 16A rms
APA100-103**	85-265Vac	385Vdc	950W	Need external Inrush current limit protection
APA100-104*	85-265Vac	385Vdc	1200W	Need external Inrush current limit protection

* 1200W at input voltage of 230Vac and above, derates to 750W at 115Vac.
** For APA100-103, 950W at input voltage of 230Vac and above, derates to 550W at 115Vac.

Safety

UL:	UL1950
CSA:	CSA C22.2 No.950
VDE:	VDE0805
	EN60950
CE:	CE Mark

Please contact Astec for information on specific module approvals.
Note: *Ensure all modules are used according to the Installation Instructions provided with each module.*
All modules are designed to meet the following specifications.

- EN55022-A(1)
- EN55022-B(1)
- VDE0871-A(1)
- VDE0878-A(1)
- IEC905
- IEC6100-44(1)
- IEC6100-45(1)
- IEC6100-3-2(1)

(1) Require additional external circuitry for full compliance. Please refer to applications section of this manual or contact technical support office for further information.

Operational Guidelines

The Power Factor Correction modules APA100 require that the following guidelines are followed to ensure reliable and correct operation.

DO

√ Ensure that control pin 9 (VADJ) is connected to pin 11 (S GND).

√ Connect an external output capacitor with a value in the range 150µF to 1200µF. (1200µF limit does not apply to APA100-103/104) Connect the capacitor as close to the output pins of the PFC as possible. The connection must be less than 50mm.

√ Use an opto-coupler when enabling AMPSS™ DC-DC converter modules using the PFC Load Enable Function (see below).

√ Use an opto-isolator or pulse transformer when connecting the CLK OUT of the PFC module to the CLK IN of AMPSS DC-DC converter module.

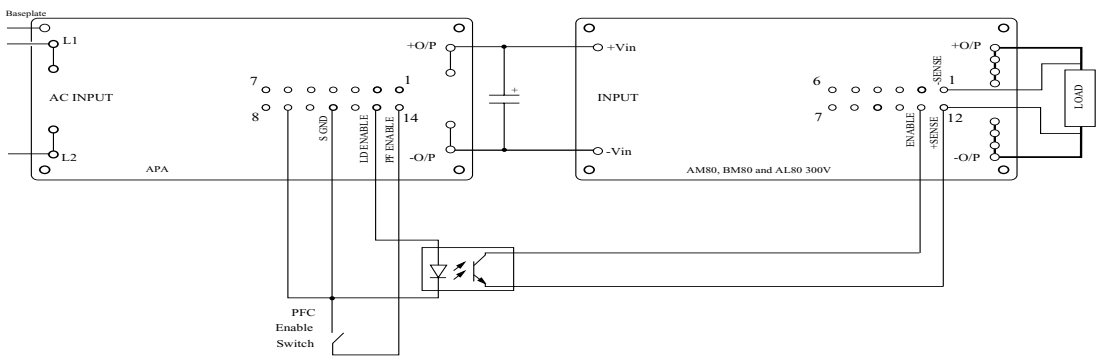
√ At 220Vac application, the PFC module cannot limit the surge current under certain missing cycle recovery condition. A surge current > 70A will demage the PFC module, please add external surge protection if necessary.

DON'T

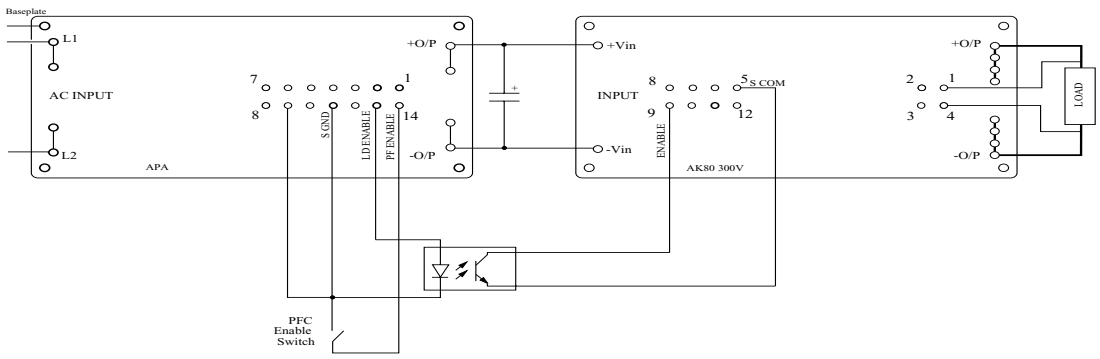
× Do not enable the load during the PFC's power up sequence. It is strongly recommended that the PFC's LD ENABLE signal be used to automatically

× Surge current must not excess 70A.

MODULE ENABLE CONNECTIONS FOR PFC TO AM80A CONVERTER



MODULE ENABLE CONNECTIONS FOR PFC TO AK80A CONVERTER



Electrical Specifications

Absolute Maximum Ratings – all models

Exceeding the specified absolute maximum ratings may severely damage the module. These ratings are intended as guidelines for absolute worst case operating conditions and are not to be interpreted as recommended operating condition

General	
Continuous Input Voltage	265Vac
Input Surge Voltage (1 sec)	290Vac
Isolation Input to Baseplate	2700VDC
Isolation, Output to Baseplate	2700VDC
Operating Temperature (Baseplate)/ Case	-20 to 85°C
Storage Temperature	-40 to 105°C
Operating Relative Humidity (non-condensing)	10% to 95%
Storage Relative Humidity (non-condensing)	95% Max
Altitude (Operating)	< 9000m
Altitude (Storage)	< 15000m
Lead Temperature (soldering 5 Seconds)	235°C

Secondary Control Pins	
TEMP MON	-0.5 to 7VDC
C MON	-0.5 to 7VDC
C SHARE	-0.5 to 7VDC
CLK OUT	-50 to 50VDC
CLK IN	-50 to 50VDC
PFW ADJ	-0.5 to 7VDC
PFW	-0.5 to 21VDC
PF ENABLE	-0.5 to 7VDC
LD ENABLE	-0.5 to 21VDC

Note : All voltages are with respect to S GND.

Specifications

Electrical characteristics are guaranteed over the full baseplate/ Case temperature range (-20 to 85°C) and for the full range of input voltage (V_I) and for the full load range (0 to I_O rated).

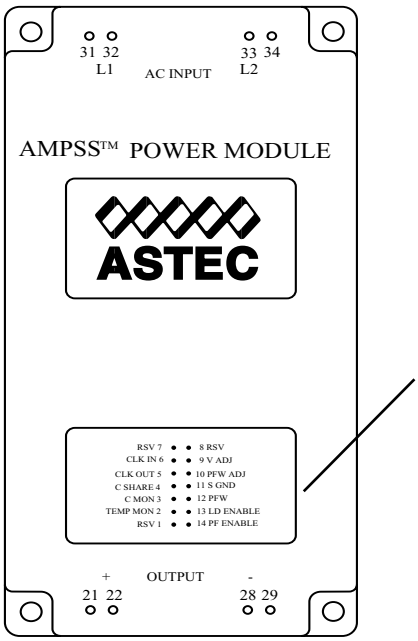
Definitions

V_I, V_O and I_O are actual operating conditions, V_{Inom}, V_{Onom} and I_{Orated} are nominal ratings.

Pin Connections - all models

INPUT PINS

Pin No	Pin Name	Type	Description	Recommended Connections
31-32	L1	Input	AC power input	Input filter or 0.47µF X-capacitor. Ensure good electrical connection and sufficient copper on PCB layouts
33-34	L2	Input	AC power input	See L1 for recommendations



CONTROL PINS

Pin No	Pin Name	Type	Description	Recommended Connections
1	RSV	-	Reserved	Leave unconnected
2	TEMP MON	Output	Provides a voltage signal proportional to the baseplate temperature of the module	Analog signal output. Leave unconnected if not used
3	C MON	Output	Provides a current signal proportional to the current being supplied by the module	Analog signal output. Leave unconnected if not used
4	C SHARE	Input/Output	Allows modules connected in parallel to accurately share current	Connect to C SHARE pins of other modules. Leave unconnected if not used
5	CLK OUT	Output	Provides a 1MHz clock output for synchronization with other modules	Capacitor coupled output. Leave unconnected if not used
6	CLK IN	Input	Accepts a 1MHz clock input for synchronization with other modules	Capacitor coupled input. Leave unconnected if not used
7	RSV	-	Reserved	Leave unconnected
8	RSV	-	Reserved	Leave unconnected
9	V ADJ	Input	Used to adjust module output voltage	Connect to S GND if not used
10	PFW ADJ	Input	Used to adjust module power fail warning threshold.	Leave unconnected for default
11	S GND	-	Ground Reference (Primary)	
12 *	PFW	Output	PFW will go from HIGH to LOW when the output power cannot be maintained at a pre-programmed level (APA 100-101/102 only)	Leave unconnected
13	LD ENABLE	Output	Enables or disables an AMPSS™ DC-DC converter	Use this signal to enable the load.
14 *	PF ENABLE	Input	Enables or disables the output of the PFC module (APA 100-101/102 only)	Must be pulled low with respect to S GND to enable the module

* Please see item C and item D on page 4 for the description of APA 100-103/104

OUTPUT PINS

Pin No	Pin Name	Type	Description	Recommended Connections
21-22	+OUTPUT	Output	Power output - positive	An external output capacitor is required
28-29	-OUTPUT	Output	Power output - negative	See +OUTPUT for recommendations

CONTROL SIGNALS

Control Function	Conditions	Parameter	Min	Typ	Max	Units
TEMP MON - temperature monitor signal		$V_{TEMP\ MON}$ Sensitivity	9.8	10	10.2	mV/°C
		Source impedence		16		KΩ
V ADJ - voltage adjust*	Adjust using external resistor	Vo	60		100	% V_{Onom}
C MON - current monitor signal	I_O = 2A	$I_{C\ MON}$	0.72	0.8	0.88	mA
	I_O = 20 to 100% I_{Orated}	$I_O/I_{C\ MON}$		2.5		A/mA
C SHARE - current share function**	C SHARE pins of modules in parallel connected	C SHARE accuracy		±3%	±10	%$I_{O\ rated}$
		Max no. of units			10	
CLK OUT - clock output		$V_{CLK\ OUT}$	3.5		5	Vp-p
	CLK IN open	Clock freq.	0.995	1	1.005	MHz
		Max fan out			2	
CLK IN - clock input		$V_{CLK\ IN}$	3.3		5.5	Vp-p
		Clock freq	0.95	1	1.05	MHz
PFW ADJ - power fail warning adjust	PFW ADJ=0 to 2.05 VDC	PFW set point	201	205	209	VDC
	PFW ADJ=3.2 VDC	PFW set point	316	320	324	VDC
	PFW ADJ ³ 3.40VDC	PFW set point	333	340	353	VDC
		PFW ADJ current source		1		mA
PFW - power fail warning***	Input Power OK, I_{PFW} = 0	V_{PFW}	15	19	21	V
	Input Power Fail, I_{PFW} = 15mA	V_{PFW}	0	0.2	0.4	V
	(PFW short to S_GND)	PFW current source	–	6	10	mA
LD ENABLE - load enable	Load enabled, ($I_{LD\ ENABLE}$ = 0)	$V_{LD\ ENABLE}$	15	19	21	V
	Load disabled, ($I_{LD\ ENABLE}$ = 15mA)	$V_{LD\ ENABLE}$	0	0.2	0.4	V
	LD ENABLE short to S_GND	LD ENABLE current source	–	6	10	mA
PF ENABLE - module enable***	Module enabled	$V_{PF\ ENABLE}$	0		0.8	V
	Module disabled	$V_{PF\ ENABLE}$	2.2		5	V
	V_{ENABLE} = 0.8V	PF ENABLE current source		50		µA

* PFW is not valid when using voltage adjust feature

** For Model APA100-101/103/104 the total input current of all the modules must not exceed 16A rms

*** PFW and PF ENABLE (Refer to item C and item D on page 5 for APA100-103/104)

Insulation - all models

INSULATION

Parameter	Conditions	Min	Typ	Max	Units
Input-baseplate insulation resistance	500VDC	10			MΩ
Output-baseplate insulation resistance	500VDC	10			MΩ

Electrical Specifications for PFC APA100-XXX

INPUT CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Units
Input voltage		85		265	Vac
Input frequency		47	50/60	63	Hz
Input low line power on voltage	Module power on				
	APA100-101/102	80		84	Vac
	APA100-103/104	70		85	Vac
Input low line power off voltage	Module shutdown				
	APA100-101/102	57		61	Vac
	APA100-103/104	55		58	Vac
No load input power	V_I = 115Vac / 230Vac			5	W
Input start-up current	V_I = 115Vac			1.4	Arms
	V_I = 230Vac			1.4	Arms
Input current	V_I = 115Vac				
	APA100-101/102/104 (Load = 750W)			9.8	Arms
	APA100-103 (Load = 550W)			7	Arms
Inrush current	For APA100-101/102				
	V_I = 115Vac		10	20	Apk
	V_I = 230Vac		18	20	Apk
	For APA100-103/104				
	With external current limit			13	A^2sec
Power Factor	V_I = 115Vac/230Vac, I_O=1A	0.96	0.97		
	V_I = 115Vac/230Vac, I_O=2A	0.98	0.99		
	V_I = 230Vac, I_O=3A	0.98	0.99		
Total Harmonic Distortion	V_I = 115Vac/230Vac			10	%

Notes :
(i) For model APA100-101/102, half cycle surge current due to input transient surge must be limited to 70A peak or less.
(II) For Model APA100-101, APA100-103 and APA100-104 total input current for modules connected in parallel must not exceed 16A.
(iii) For Model APA100-102 negative rail input rectifiers must be provided by external circuitry.
(iv) Total harmonic distortion - Input harmonics meet the requirements of IEC 1000-3-2

TRANSIENT CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Units
Turn-on time	Load must be disabled DURING POWER UP SEQUENCE Output capacitor = 470µF				
	VI = 115Vac	1.5	1.8	2.8	Sec
	VI = 230Vac	2.3	3.1	3.6	Sec

OUTPUT CHARACTERISTICS

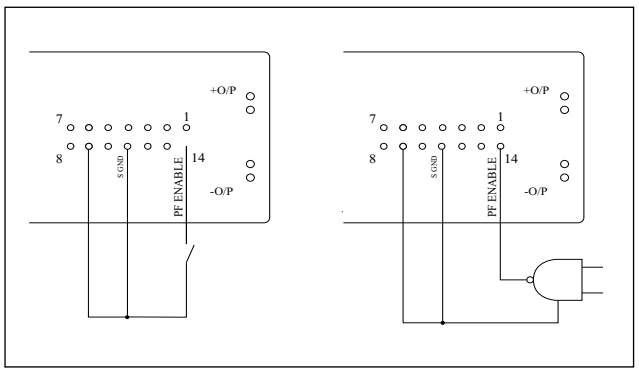
Parameter	Conditions	Min	Typ	Max	Units
Output voltage	For APA100-101/102/104				
	I_O = 3.2A / V_I > 180V	370	377		V
	I_O = 2A	375	383		V
	I_O = 0		393	400	V
	For APA100-103				
	I_O = 2.4A / V_I > 180V	370	380		V
	I_O = 1.5A	375	385		V
	I_O = 0			400	V
Output voltage adjust	PFW is invalid	60		100	% V_{Onom}
Maximum output power	For APA100-101/102/104				
	85Vac ≤ VI ≤ 120Vac			750	W
	120Vac < VI < 220Vac		see page 15		
	VI³ 220Vac			1200	W
	For APA100-103				
	V_I = 85 Vac			550	W
	V_I = 230Vac			950	W
Output overvoltage shutdown (latch off)		410	417	425	V
Overtemperature shutdown (latch off)	For APA100-101/102/104				
	Baseplate temperature	85	90	95	°C
	For APA100-103				
	Baseplate temperature	85	95	100	°C
Efficiency	For APA100-101/102/104				
	VI = 115Vac, (750W)	90	92		%
	VI = 230Vac, (750W)	92	94		%
	VI = 230Vac, (1200W)	92	95		%
	For APA100-103				
	VI =115Vac, (550W)		90		%
	VI = 230Vac, (550W)		92		%

NOTE :
An output hold-up capacitor must be added externally - see under Design Considerations.

Functional Description

This section explains how to implement the functions found on the APA100 Power Factor Correction Series.

PFC Enable Input (PF ENABLE)



For APA100-101/102

The enable pin is a TTL compatible input used to turn the output of the module on or off. The module output is enabled when the PF ENABLE (pin 14) is connected to S GND (pin11) or driven to a logic low of <0.8V (but not negative).
The output is disabled when the enable pin is open or driven to a logic high >2.2V. All monitoring and house-keeping functions (including clock signals) continue to operate normally.

For APA100-103/104

The function of the PF ENABLE has changed. With the PF enabled the output is Power Factor corrected and boosted. With PF disabled the output is AC input voltage rectified.

S GND (Signal Ground)

The S GND pin is connected to the internal common ground of the module. It is also internally connected to the -O/P terminals.

NOTE:
When connecting S GND to external circuitry care must be taken to ensure that the current flowing through this pin is kept below 25mA.

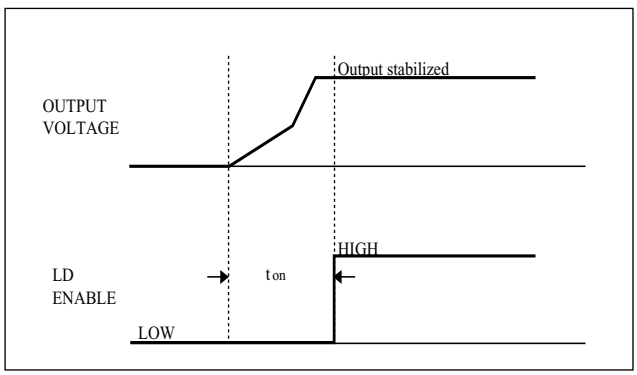
Protection against short circuit before power-on

(Does not apply to APA100-103/104)

After the module is enabled, if the output does not rise above 20V in 400msec a short circuit condition is assumed to exist and the module will shut down. Once the short circuit condition is removed the module can be restarted by toggling the input or the PF ENABLE off then on again.

DC-DC Converter Module Enable Output (LD ENABLE)

After the PFC power up sequence, the power to the load can be enabled. This can be performed manually or the PFC can automatically enable the load using the LD ENABLE signal.

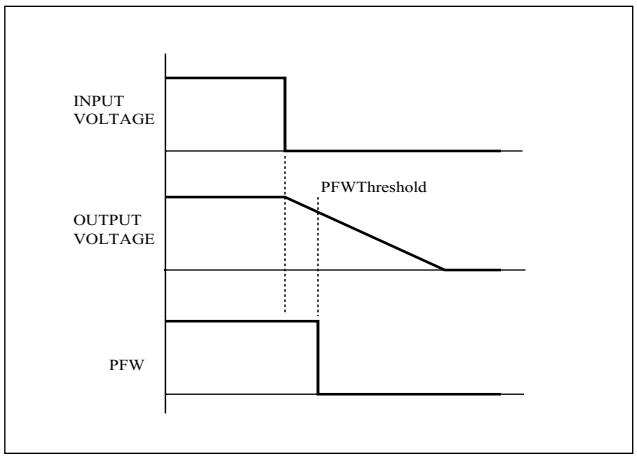


Initially, the load is disabled and the LD ENABLE (pin 13) is at 0.4V (LOW). When the PFC power up sequence has completed, the LD ENABLE voltage goes HIGH.. The LD ENABLE pin is capable of delivering 3.5mA at 1.5V when HIGH. See electrical specifications for exact figures.

NOTE:
If the load is to be enabled manually it is essential that the PFC has completed its power up sequence before enabling.

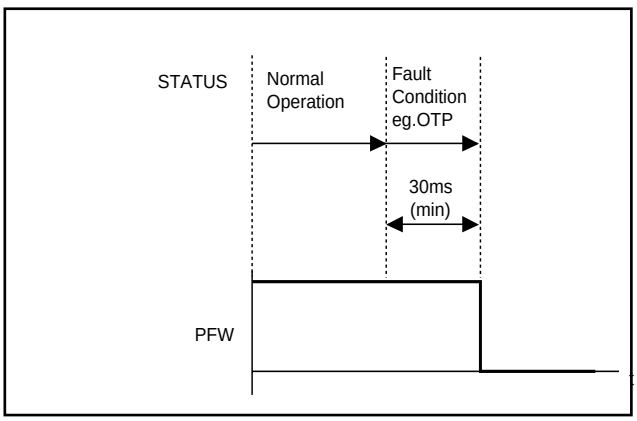
Power Fail Warning

If the input voltage should drop to a level such that output power can not be maintained, then the PFW (pin 12) will go from HIGH to LOW at a pre-programmed PFW threshold output voltage.



The output of the PFW signal can be used to signal to system logic that the input power is failing. It can direct drive an opto-coupler to provide an isolated signal for the secondary side. The nominal factory set PFW threshold is set at 340V.

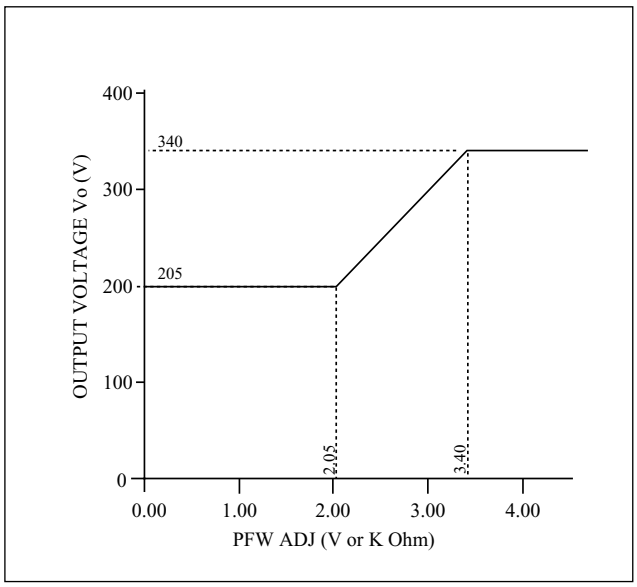
For APA100-103/104, the PFW will go from HIGH to LOW also when a fault condition occur (OTP, OVP and general fault conditions) or if PFC is disabled using the PF Enable function.



When a condition occurs to trigger the PFW function there is a minimum delay of 30ms (100ms typical) before the PFW signal goes from High to LOW.

Power Fail Warning Adjust

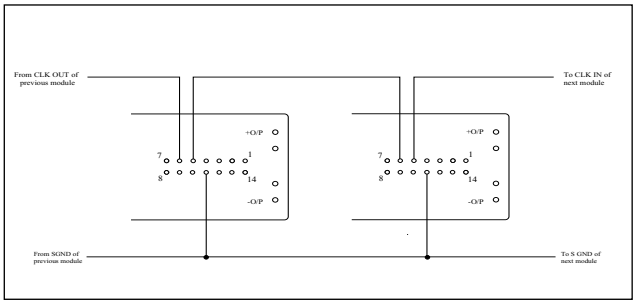
The level at which a Power Fail Warning occurs can be programmed using the PFW Adjust input (pin 10). If the pin is left unconnected then the PFW operates at the default factory set value.



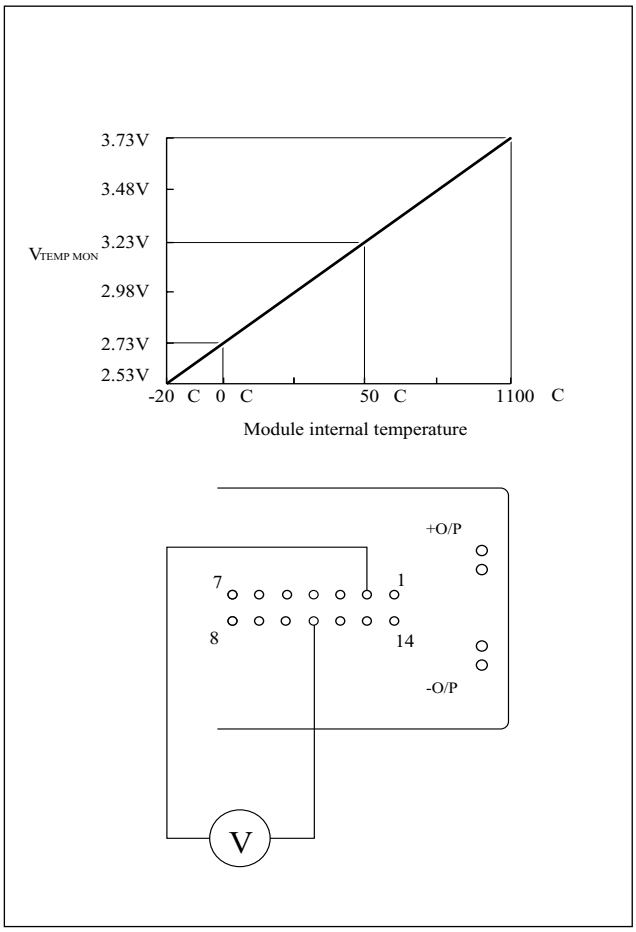
The output from the PFW ADJ pin is a 1mA current source. To adjust the PFW threshold, a voltage source (0-4 Volts) or a programming resistance (0-4 kOhm) referenced to S GND (pin 11) should be connected. This allows adjustment of the PFW threshold from 205V up to 340V. The value of resistance or voltage required can be read from the graph above.

Clock Signals (CLK IN , CLK OUT)

The PFC's internal clock is accurate and stable over its full operating range. Synchronization is not normally required but it can reduce noise in paralleled systems.
Clock signals can be wired in series (the CLK OUT (pin 5) of one module to the CLK IN (pin 6) of the next etc.) in which case all the modules will be synchronized with the first module in the chain. Alternatively, an external clock signal of 5Vpk-pk at 1MHz±5% can be connected to the CLK IN pins of all the modules.
If the clock input to any module fails, the module will automatically switch back to its internal clock and will



continue to operate at full power even in current sharing systems. The CLK IN and CLK OUT signals are AC coupled.



Temperature Monitoring (TEMP MON)

The TEMP MON (pin 2) provides an indication of the module's internal temperature.The voltage at the TEMP MON pin is proportional to the temperature of the module interior at 10mV per °C (or K).
Therefore the module temperature can be read directly as :

$$\text{Module temperature (K)} = V_{\text{TEMP MON}} \text{ (Volts)} \times 100$$

or converted to °C where;

$$°C = K - 273$$

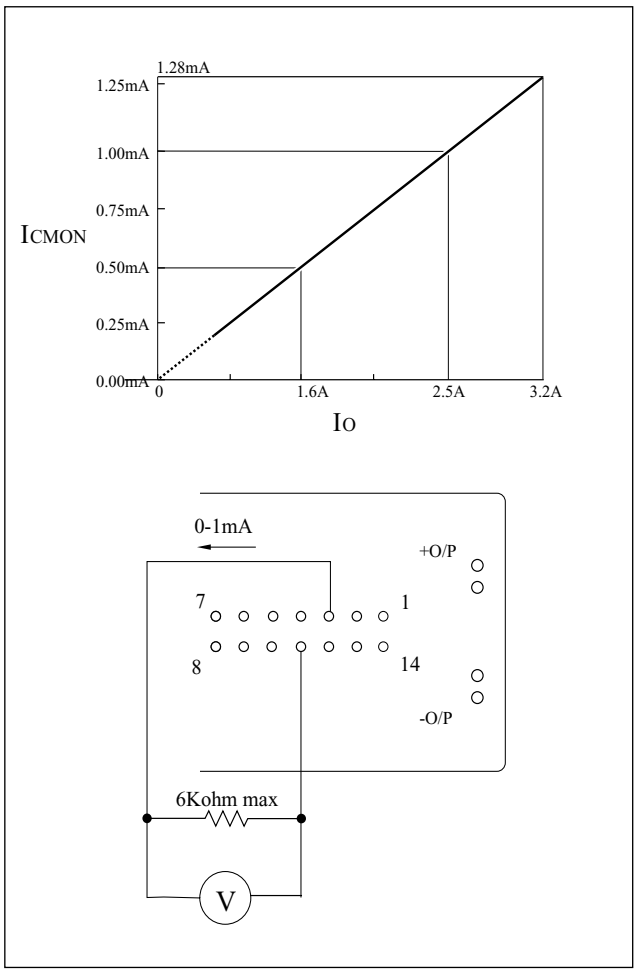
The temperature monitor signal can be used by thermal management systems (e.g. to control a variable speed fan). It can also be used for overtemperature warning circuits and for thermal design verification of prototype power supplies and heatsinks.

Current Monitoring (C MON)

The C MON (pin 3) provides an indication of the amount of current supplied by the module. The output of the C MON pin is a current source proportional to the output current of the module,
where :

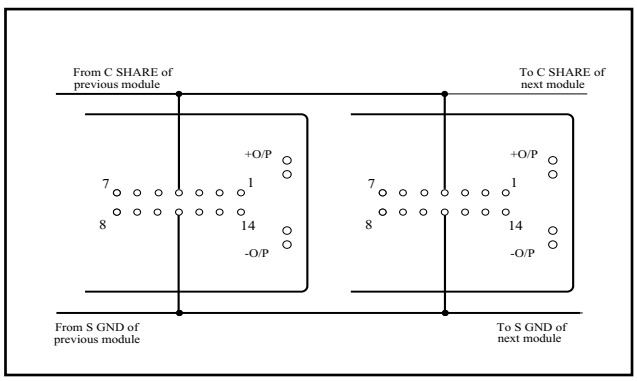
$$I_O/I_{C\,MON} = 2.5A/1mA.$$

If a 2.5 KOhm resistor is connected then the voltage in Volts on the C MON pin is directly equivalent to the current supplied by the module in Amps.



The C MON output can be paralleled with C MON outputs from other modules to indicate the total current supplied in a paralleled system.

Current Sharing (C SHARE)

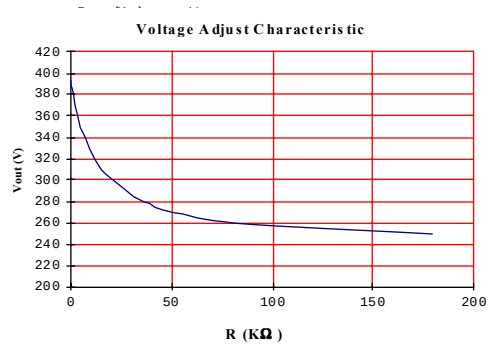


To ensure that all modules in a parallel system accurately share current, the C SHAREs (pin 4) should be connected together as shown.
The voltage on the C SHARE pins represents the average load current per module. Each module compares this average with its own current and adjusts its output voltage to correct the error. In this way the module maintains accurate current sharing even under variable or light load conditions.

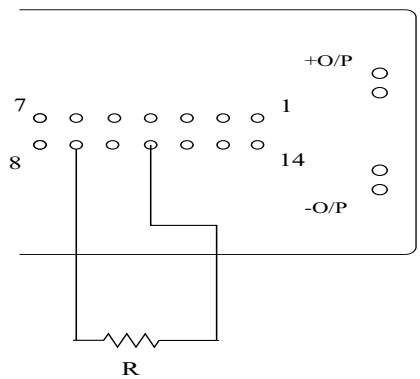
Note:
The S GND pins of each module must also be connected together to ensure accurate current sharing.

Output Voltage Adjust (V ADJ)

The output voltage of the module may be accurately adjusted from 60% to 100% of the nominal output voltage. Adjustment can be made using a resistor connected as below.



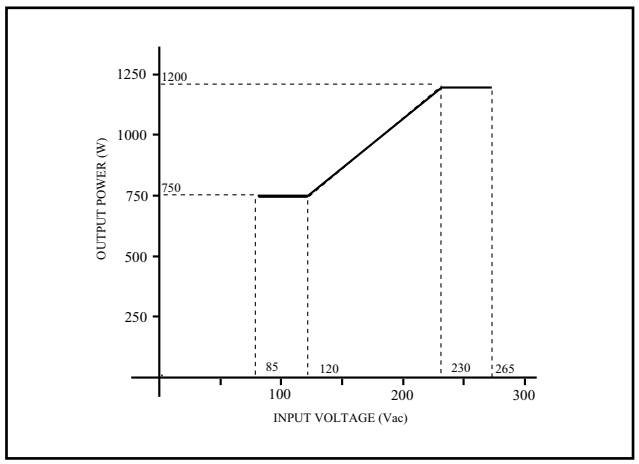
If V_{in} = 115V_{AC}, output voltage ADJ range is 240 to Vo(nom)
If V_{in} = 220V_{AC}, output voltage ADJ range is 330 to Vo(nom)



Design Considerations

Maximum Output Power Vs Input Voltage

The maximum output power available varies with the input voltage as shown below.



Input Undervoltage Protection

An input undervoltage protection circuit protects the module under low input voltage conditions. Hysteresis is built into the PFC Series module to allow for high levels of variation on the input supply voltage without causing the module to cycle on and off. PFC modules will turn on when the input exceeds 85Vac and turn off below 63Vac. (see Electrical Specifications for exact figures).

Input Fusing

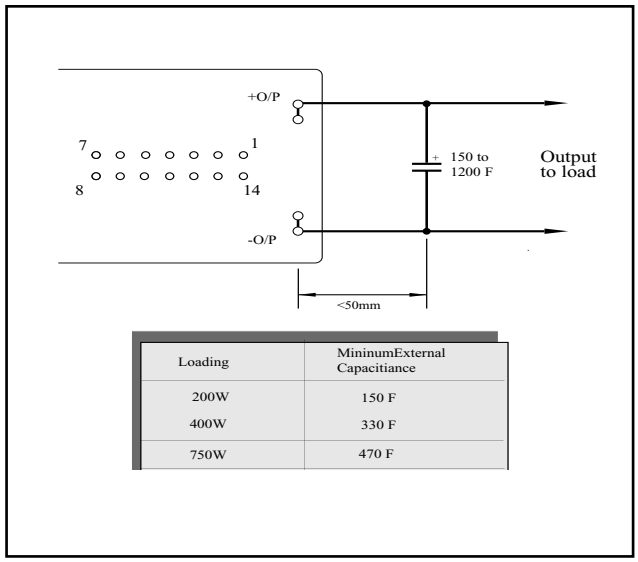
AMPSS modules do not have an in-line fuse fitted internally. In order to comply with CSA, VDE and UL safety regulations it is recommended that a fuse of the following rating be fitted at the module's input.

Input	Fuse Rating
300	15A / 250V

Output Capacitor

NOTE:
The PFC requires an output hold-up capacitor of between 150µF and 1200µF(1200µF limit does not apply to APA100-103/104) to prevent the module from disabling due to fluctuations in output voltage.

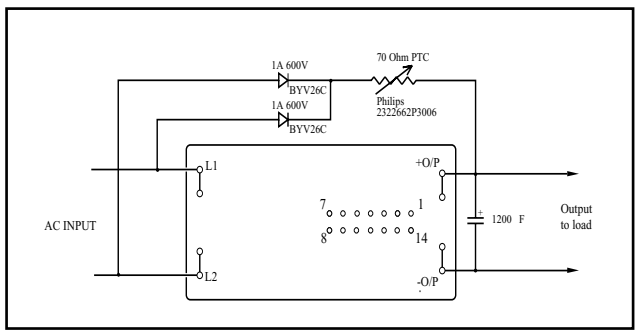
Ideally the capacitor should be connected directly to the PFC output pins. If this is not possible the connection must be less than 50mm from the pins.



Loading	MininumExternal Capacitiance
200W	150 F
400W	330 F
750W	470 F

Charging of Output Capacitor

For large values of external output capacitance and for loads, which when disabled draw stand-by currents > 150mA, a charging circuit is recommended.
For example, the circuit diagram shown below is for an input of 264Vac with an output capacitor of 1200µF.



Selecting an External Output Capacitor

The output capacitor value is determined by the following factors :
1. RMS ripple current.
2. Peak-to-peak output ripple voltage.
3. Hold-up time.
4. Expected lifetime of the capacitor.

RMS ripple current
The maximum permissable rms ripple current for the output capacitor should be greater than the rms ripple current for the application. The ripple current for the APA100 PFC module can be approximated as

$$I_{rms} = (P_O/Eff) \times 1/\sqrt{(V_O \times V_{rms})}$$

where :
P_O = output power (W)
Eff = efficiency
V_O = output voltage (V)
V_{rms} = input rms voltage (V)

This gives the ripple current at 125KHz. The maximum ripple current for capacitors is usually specified at 120Hz. To convert from 125KHz to 120Hz the Irms figure should be divided by 1.3 .

Peak to Peak Output Ripple Voltage
The ac input causes a ripple on the output voltage. The size of the ripple is inversely proportional to the size of the capacitor. Therefore the maximum allowable ripple voltage should be decided in order to calculate the size of capacitor required. This may be calculated using the following equation :

$$C_O = P_O / (2pf \times Eff \times V_O \times V_{ripple})$$

where :
C_O = output capacitance (µF)
Eff = efficiency
f = input voltage frequency (Hz)
V_O = output voltage (V)
V_{ripple} = output ripple voltage (V)

Hold-Up Time Requirement
The output capacitor value is different for different hold-up time requirements. The minimum capacitance corresponding to the required hold-up time of a system comprised of AMPSS DC/DC power modules and an APA100 PFC module can be calculated as follows :

$$C_{O\,min} = (2 \times P_O \times T_{hold})/[(V_O - V_{ripple})^2 - (V_{min})^2]$$

where :
$C_{O\,min}$ = output capacitance (µF)
P_O = output power (W)
T_{hold} = hold up time (sec)
V_O = output voltage (V)
V_{ripple} = output ripple voltage (V)
V_{min} = minimum input voltage for DC/DC module

For example :
A PFC APA100-101 module driving 3*AMPSS*™ AM80A 200W modules @ 5V. Efficiency of the AM80A module is 84%, the minimum input voltage is 180V, the output voltage of the PFC is 380V, the required hold-up time is 20mS and the peak-to-peak voltage V_{ripple} is chosen to be 15V.

$$C_{O\,min} = \frac{2 \times (3 \times 200/0.84) \times 0.02}{[(380-15)^2 - 180^2]} = 283\mu F$$

This figure is the minimum capacitance. To allow for capacitor tolerences and ageing effects the actual value should generally be around 1.5 times greater.

Expected Lifetime of the Capacitor
The lifespan of a capacitor is dependent on the temperature. The electrolyte dries up faster at higher temperatures. The lifespan of the capacitor can be calculated using the equation shown.

$$L = L_{rated} \times 2^{[T_{rated} - T_{int})]/10}$$

where :
L = lifespan at T_{int} (hrs)
L_{rated} = min. useful life at rated temperature & voltage (hrs)
T_{rated} = rated maximum temperature (°C)
T_{int} = the internal temperature of the capacitor (°C)

Generally the internal temperature rise of the capacitor will be 1.4 to 2 times the external temperture rise of the capacitor. The internal temperature rise can be calculated using the equation below :

$$T_{int\_rise} = (I_{OP}/I_{SP})^2 \times T_{ext\_rise}$$

where :
T_{int_rise} = internal temperature rise
T_{ext_rise} = external temperature rise
I_{OP} = operating rms ripple current
I_{SP} = is the rated maximum rms ripple current

For example -
Ripple current of 3A measured at 120Hz and a rated maximum ripple current of 1.76A. External temperature rise is measured at 4°C over an ambient temperature of 40°C. If the minimum useful life of a 470µF/450V capacitor is specified at 2000Hrs @ 105°C then the expected useful life of the capacitor is calculated as :

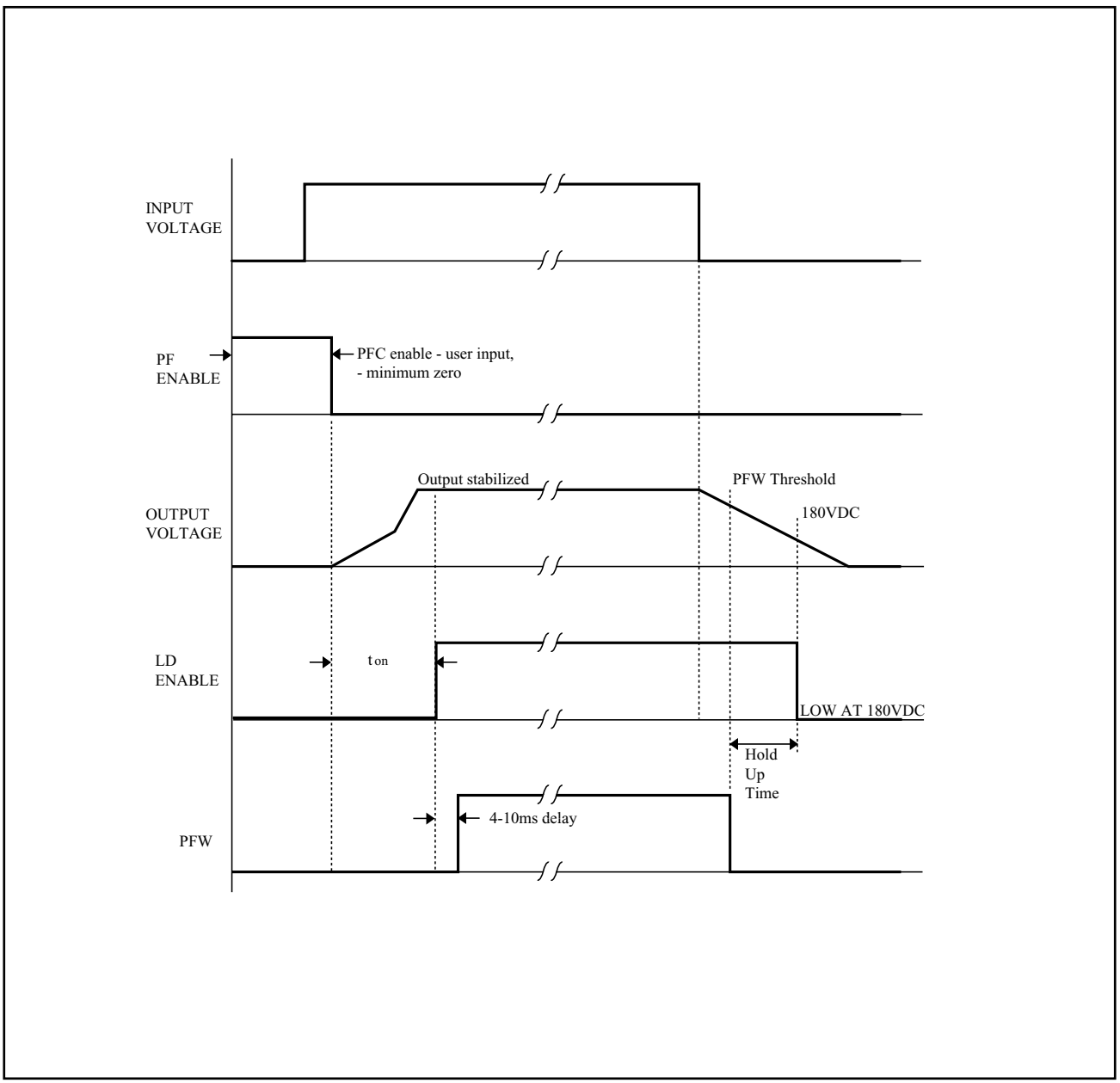
$$L = 2000 \times 2^{[105-(40+14.5)]/10} = 66{,}257 \text{ Hrs}$$

PF & Load Enable Connections and Timing

Timing of LOAD ENABLE

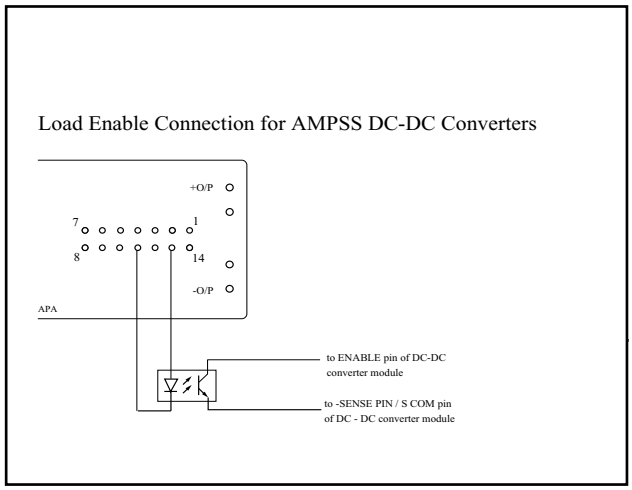
The PFC module must be supplied with a PF ENABLE signal to initiate the start-up sequence. The output of the LD ENABLE pin goes HIGH (ON) once the PFC has completed its start-up sequence.

NOTE:
It is recommended that the LD ENABLE signal is always used to enable the load, however, if the load is to be enabled manually it is essential that the t_{on} time has expired before enabling occurs.



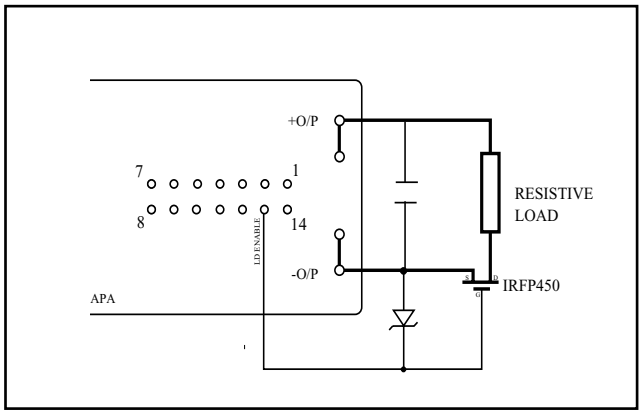
Connections to enable AMPSS™ DC-DC converters.

The output from the PFC's LD ENABLE (pin 13) can directly drive an opto-coupler to provide an isolated signal to enable the power output of one or more AMPSS™ DC-DC converter modules.



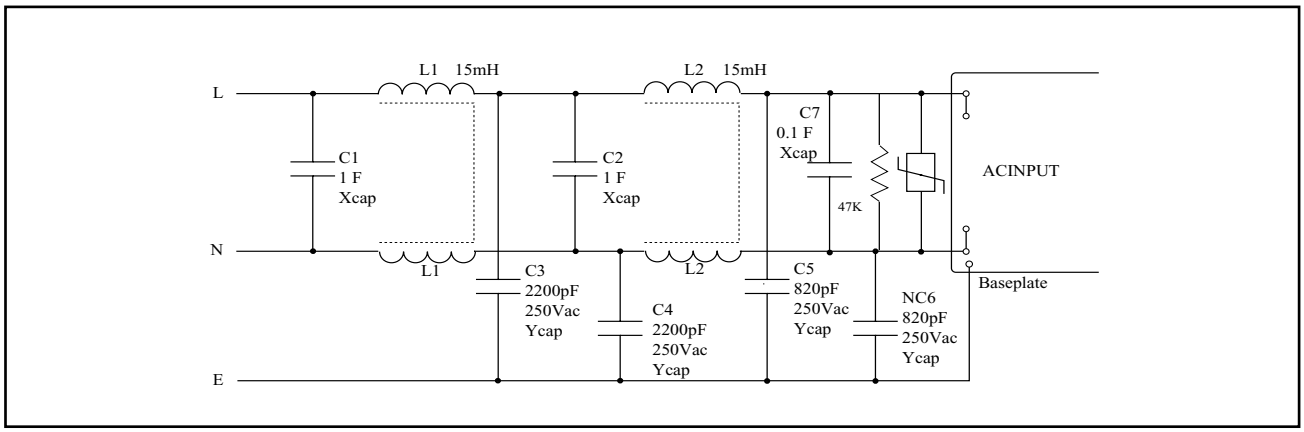
General Connections to enable a load.

For enabling loads other than AMPSS™ DC-DC Converters the following circuit can be used. The LD ENABLE pin can directly drive a MOSFET with a 15V zener clamping the gate voltage.



Conducted EMI

AMPSS™ PFC modules will require additional EMI filtering to enable the system to meet relevant EMI standards.
PFC modules have an effective input to ground (baseplate) capacitance of 1600pF. This should be accounted for when calculating the maximum EMI 'Y' capacitance to meet ground leakage current specifications. An example filter circuit is shown below.



Model APA100-101 Parallel Operation

Maximum Input Current

The APA 100-101 may be used in paralleling applications where the maximum total input current does not exceed 16A rms. For applications requiring an input current greater than 16A rms the APA100-102 should be used.

Connections

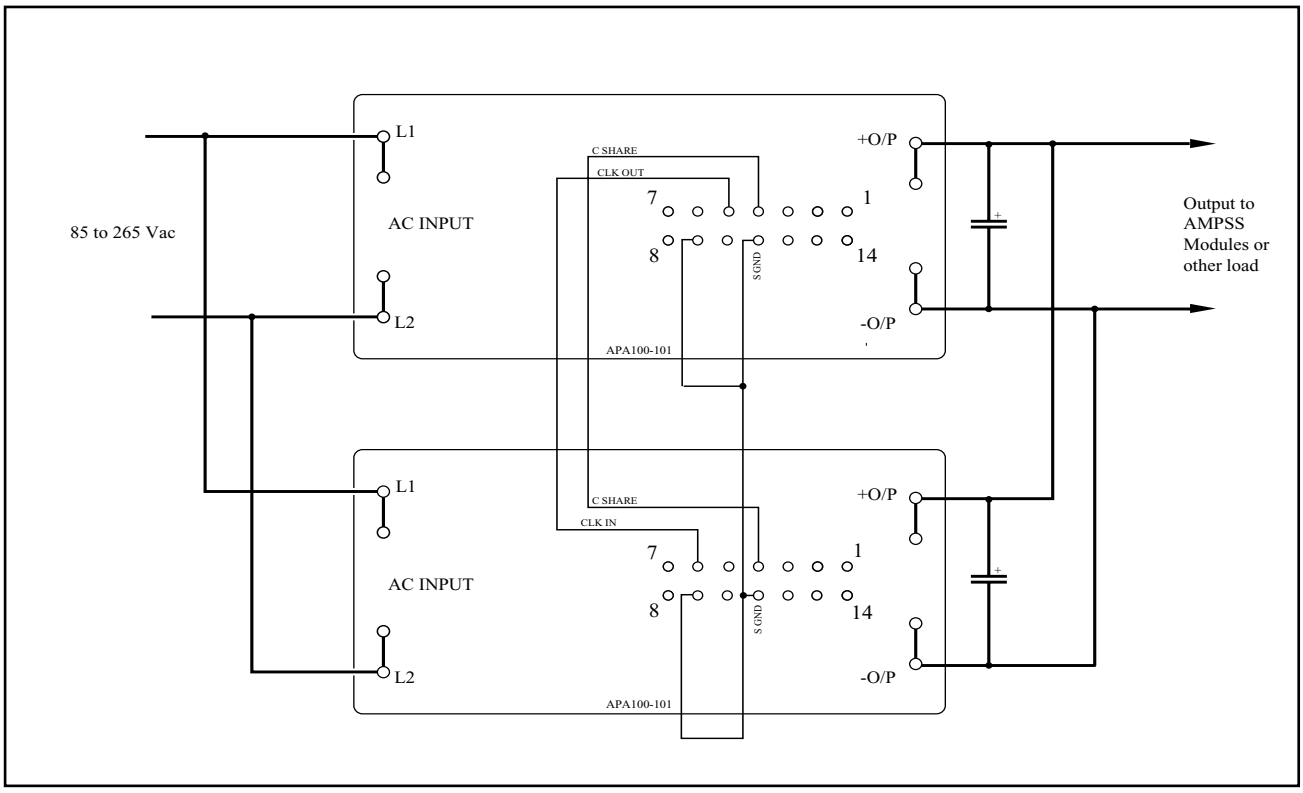
A master slave configuration is not required for AMPSS™ modules. PFC modules may be connected in parallel using a simple, single wire connection.

Current Sharing

In multi-module paralleled systems, all modules will share current to within ±3% (typical) of the average load current when the C SHARE pins of each module are connected together.

Synchronization

Modules are synchronised by connecting the CLK OUT pin of one module to the CLK IN pin of the next in an open daisy chain configuration. If the clock input to a module fails it will automatically revert to its internal clock and continue to operate at full power.



Model APA100-102 Parallel Operation

APA100-102 Applications

The APA 100-102 has been specifically designed for paralleling applications where the total input current exceeds 16A rms. For stand-alone applications or those where the total input current does not exceed 16A rms the APA100-101 is recommended.
The APA100-102 requires external negative rail rectifiers to be implemented at the input to the system. It is possible to operate the APA100-102 as a stand-alone configuration although the external negative rail rectifiers must still be provided.

Connections

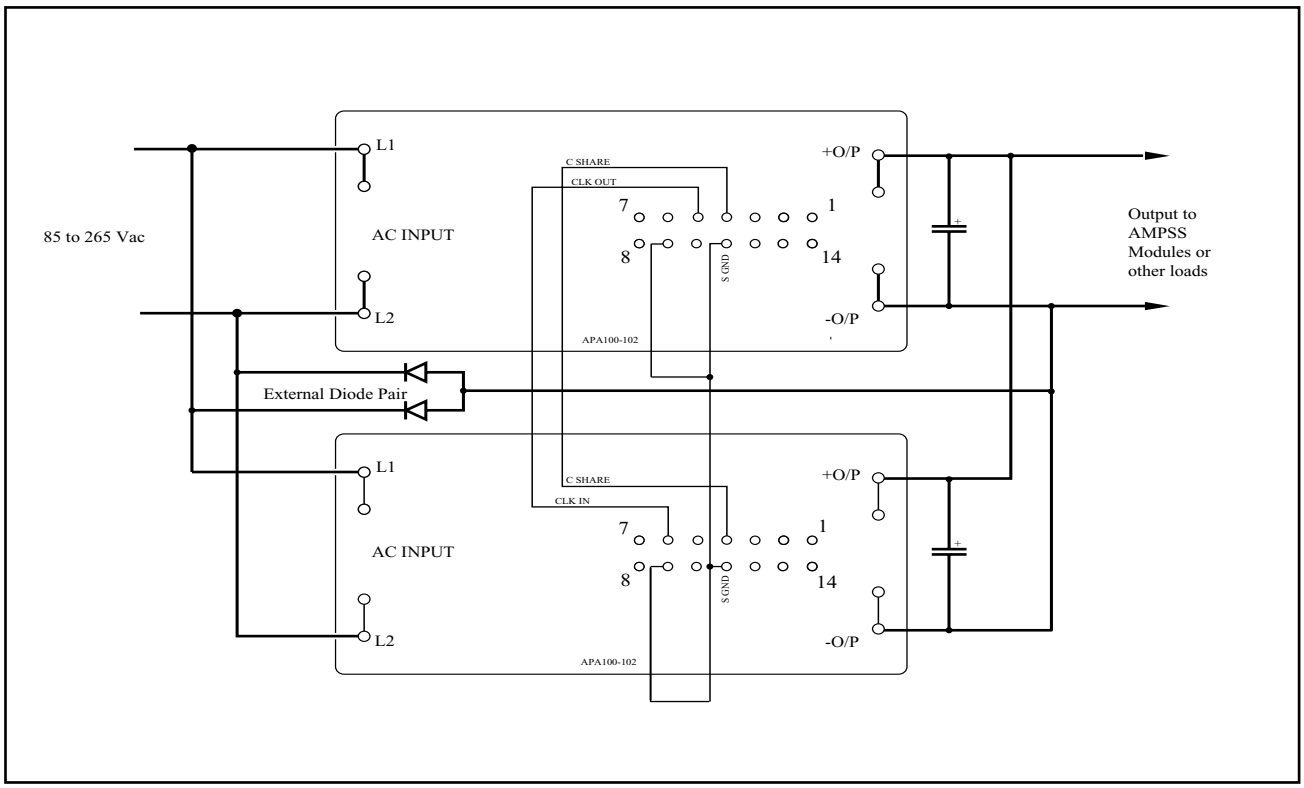
A master slave configuration is not required for AMPSS™ modules. PFC modules may be connected in parallel using a simple, single wire connection with external diode pair.

Current Sharing

In multi-module paralleled systems, all modules will share current to within ±3% (typical) of the average load current per module when the C SHARE pins of each module are connected together.

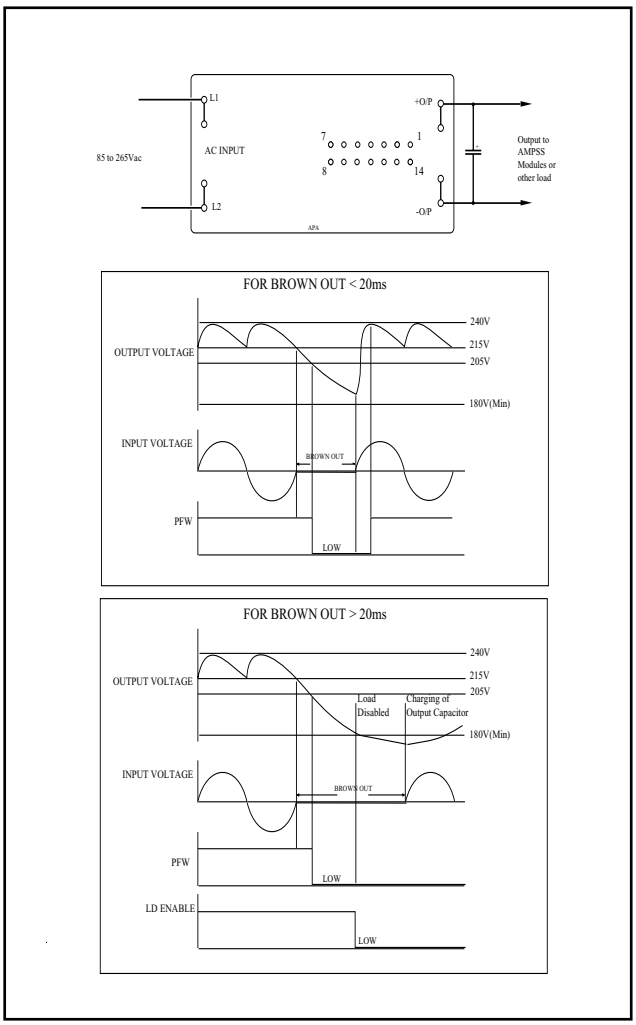
Synchronization

Modules are synchronised by connecting the CLK OUT pin of one module to the CLK IN pin of the next in an open daisy chain configuration. If the clock input to a module fails it will automatically revert to its internal clock and continue to operate at full power.



Brown Out Ride Through

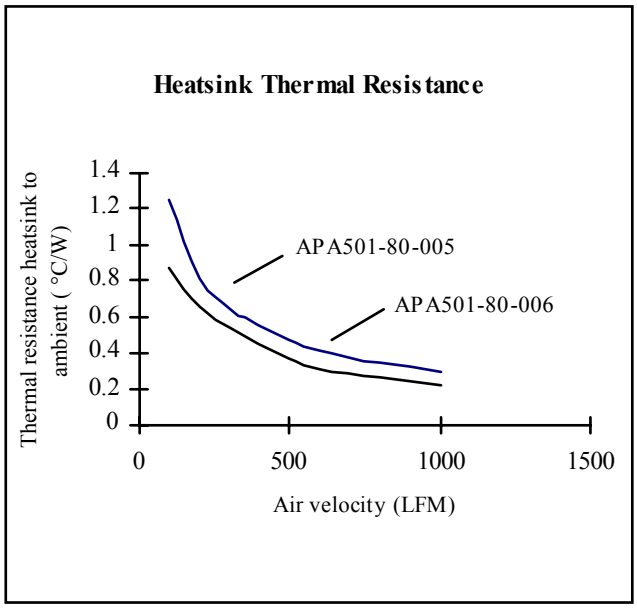
Brown Out conditions occur when there is a transient break in input current. During this period the external output bulk capacitor holds up the voltage to the load until input current is restored. When the input voltage is restored the PFC module will continue delivering power to the load



After a Brown Out condition where the output voltage has not dropped below 180Vdc, the module will recover when input power is restored.
The PFW signal can be used to monitor input power loss.

Thermal Data

Natural convection thermal impedance of the PFC package without a heatsink is approximately 4°C/W.
A standard horizontal fin heatsink available from Astec (part number APA501-80-006) with 37mm fins and 8.8mm pitch, will reduce module thermal impedance to 0.4°C /W with a forced air flow of 2.5 m/s (500 LFM) when mounted with a thermal pad (ASTEC P/N APA502-80-001) between heatsink and module.

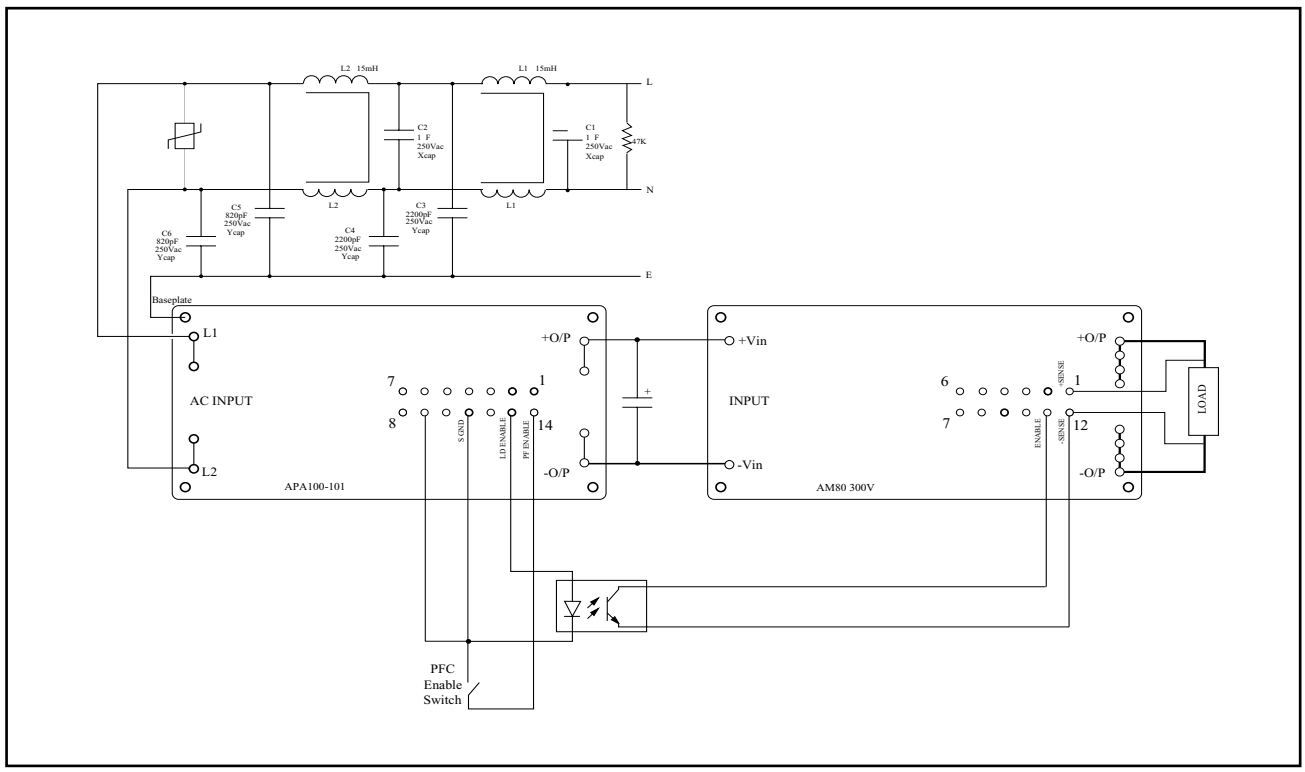


Overtemperature Protection

If the module's internal temperature exceeds 90°C (typical), the module will protect itself by latching off

Application Examples

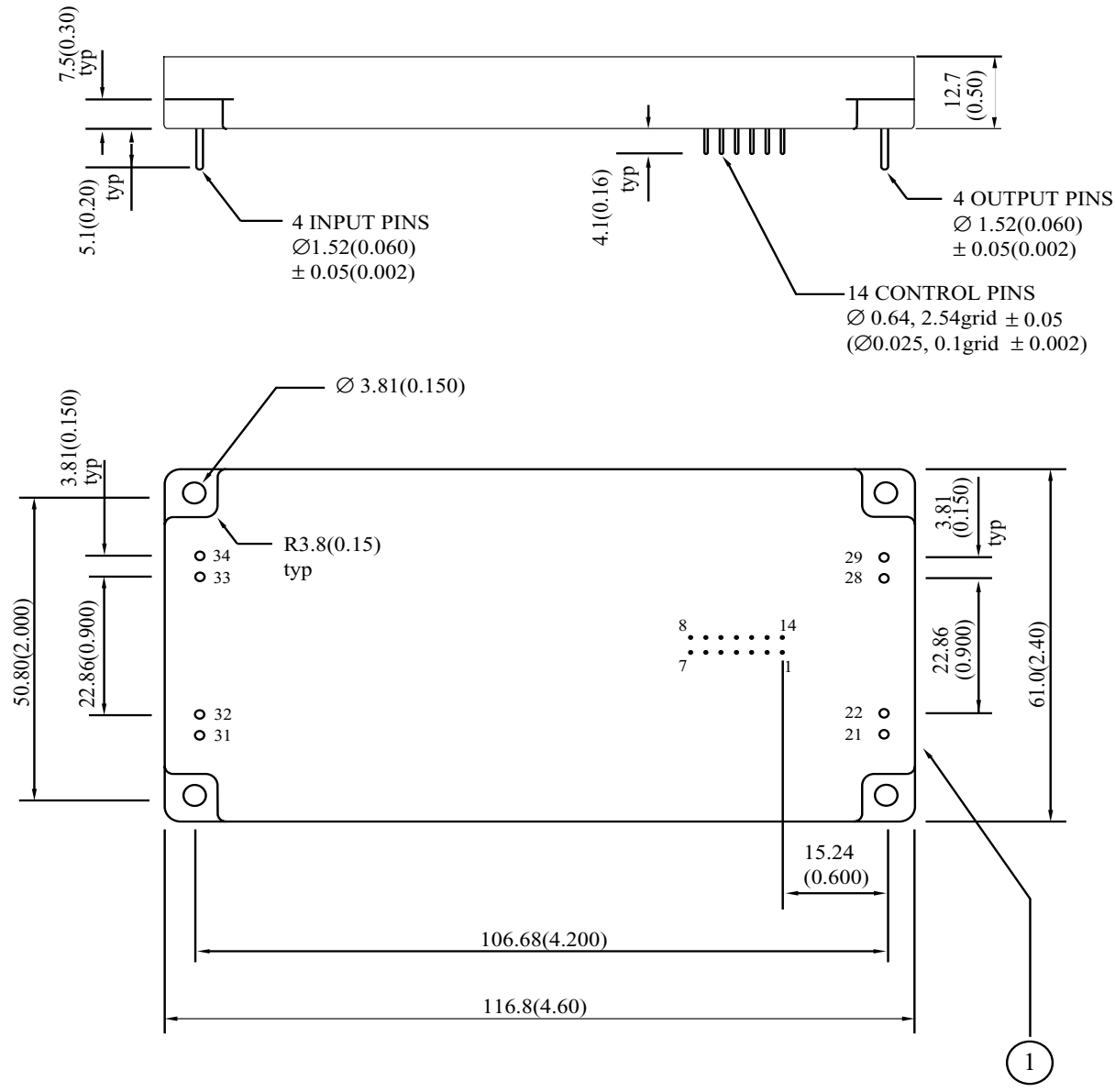
PFC Module Controlling an AMPSS™ DC-DC Converter



Mechanical Information

Dimensions

The dimensions are given in mm (inches). Note that the baseplate must be connected to protective earth before power is supplied to the module.



Notes:
1. All dimensions in mm and (inches)
2. General tolerance: .X ± 0.5(0.02)
   .XX± 0.25(0.010)
3. Surface Flatness: Concave 0.12mm max
   Convex 0.38mm max

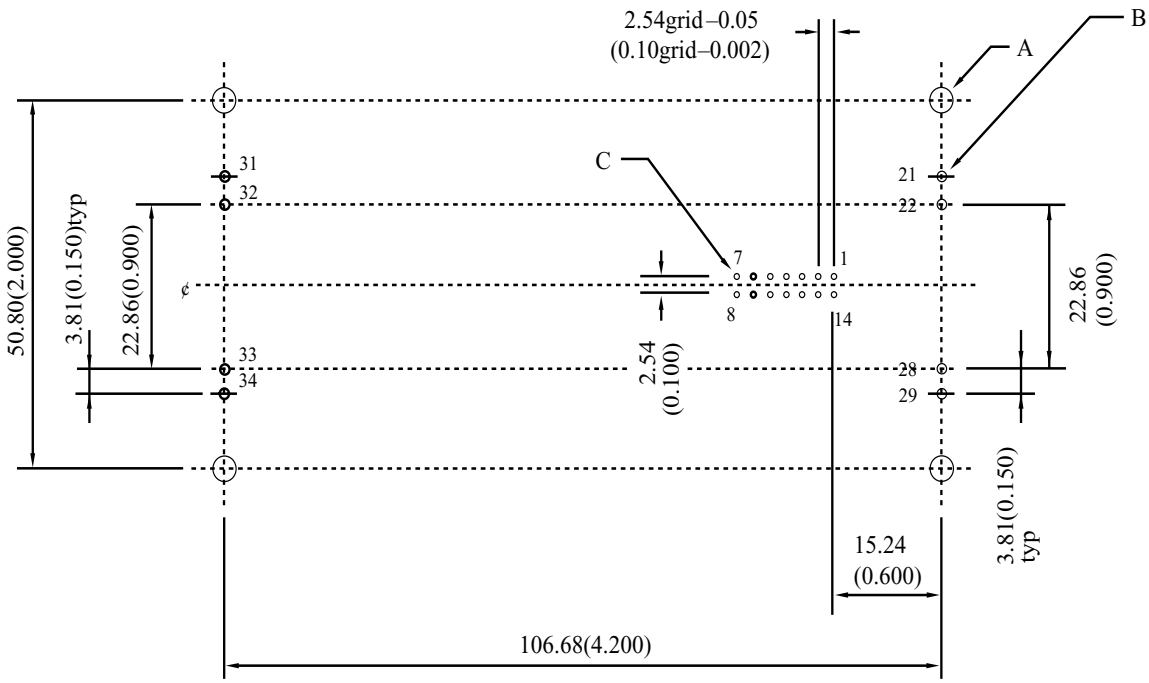
Label description ◯

1 Serial number label

Recommended PCB Layout

The APA100 Power Factor Correction Series module may be mounted to a board either by soldering or by using spring sockets.

Materials :
Control pins are tin plated phospher-bronze.
Input and output pins are tin plated copper.



VIEW FROM PCB COMPONENT SIDE

NOTES:
1. PCB COMPONENT SIDE VIEW IS SHOWN.
2. ALL DIMENSIONS IN mm AND (INCHES).
3. GENERAL TOLERANCE: .XX – 0.1(0.006).

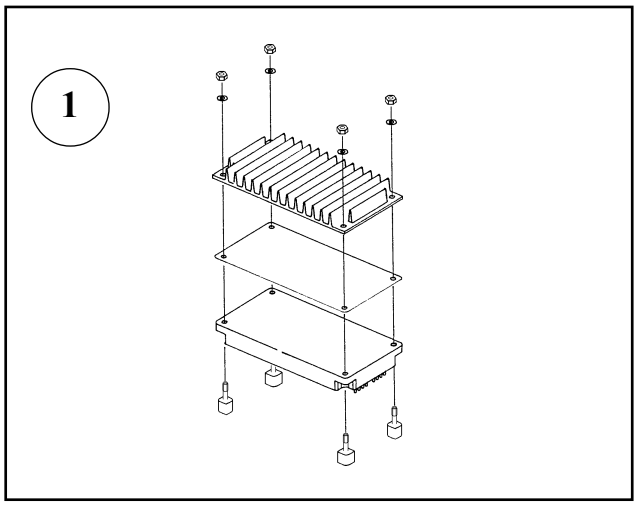
RECOMMENDED HOLE SIZE TABLE: -

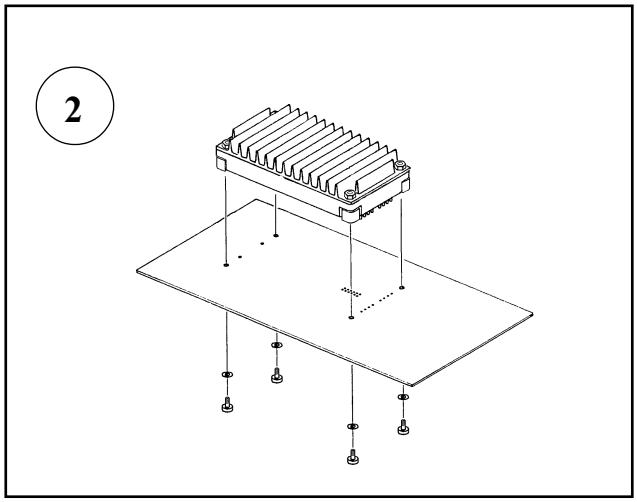
	A	B	C
HOLE SIZE FOR PCB DIRECT SOLDERING	∅ 2.00 + 0.15/-0 (∅ 0.079 + 0.006/-0)	∅ 2.00 + 0.15/-0 (∅ 0.079 + 0.006/-0)	∅ 1.00 + 0.15/-0 (∅ 0.039 + 0.006/-0)
HOLE SIZE FOR SPRING SOCKET MOUNTING*		∅2.67 ±0.05 (∅ 0.105 ± 0.002)	∅ 1.37 ±0.05 (∅ 0.054 ± 0.002)
HOLE SIZE FOR M3.5 MACHINE SCREW	∅ 4.5 + 0.08/-0 (∅ 0.177 + 0.0031/-0) FORM 3.5		

*Spring sockets are available from Astec in packs of 20 control pin sockets and 15 power pin sockets, part no. APA504-00-001. Sockets are not suitable for output current greater than 10A per pin.

Heatsink Mounting Information

Heatsinks for AMPSS™ modules are available in a variety of sizes and fin orientation. Mounting kits and thermal pads are also available. The table below shows the options available for APA100 Power Factor Correction Series.
A heatsink mounting kit provides the most convenient way to mount the heatsink to the module and then mount AMPSS™ modules may be retained by their input and output pins only, or may be fixed to the board using bolts screwed into the tapped studs which are provided as part of the mounting kit. In both cases the studs provide clearance between the module and the circuit board to facilitate PCB cleaning operations.





Note: *1) Baseplate and heatsink must be connected to protective earth*
2) Mechanical support must not induce twist in the module baseplate and must incorporate strain relief, e.g. spring washers.

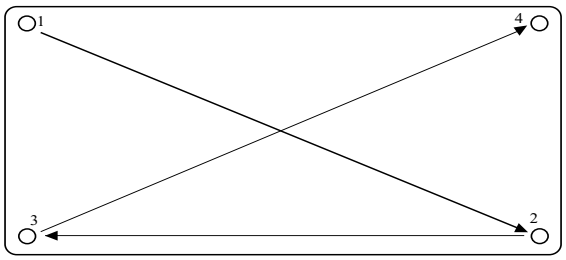
Description	Model Number	Dimensions		Free air thermal resistance
		inches	mm	
Heatsink, "80" size, vertical fin.	APA501-80-001	4.53x2.32x0.6	115x59x15	2.7°C/W
Heatsink, "80" size, horizontal fin	APA501-80-002	4.53x2.32x0.6	115x59x15	2.4°C/W
Heatsink, "80" size, vertical fin.	APA501-80-003	4.53x2.32x0.9	115x59x22.5	2.2°C/W
Heatsink, "80" size, horizontal fin	APA501-80-004	4.53x2.32x0.9	115x59x22.5	2.0°C/W
Heatsink, "80" size, vertical fin.	APA501-80-005	4.53x2.32x1.5	115x59x37	2.0°C/W
Heatsink, "80" size, horizontal fin	APA501-80-006	4.53x2.32x1.5	115x59x37	1.7°C/W
Heatsink, "80" size, low profile	APA501-80-007	4.55x3.50x0.5	115.6x89x12	2.2°C/W
Thermal Pad, "80" size	APA502-80-001			
Mounting Kit, Tapped Studs	APA503-00-001			
Mounting Kit, Solder Studs	APA503-00-002			
Mounting Kit, Tapped Studs for low profile heatsink	APA503-00-007			
Mounting Kit, Solder Studs for low profile heatsink	APA503-00-008			
Spring Sockets (20 cont. 15pwr)	APA504-00-001			

To provide optimal thermal contact between heatsink and module, it is recommended that the mating surface of the heatsink should have a surface flatness of no greater than 0.1mm. The use of a thermal pad or thermal grease is also recommended.

The recommended torque of using AMPSS mounting kit for module/heatsink is:

Screw size	Torque
M3	4-6kg-cm (3.5-5.2lb-in)
M3.5	6-8kg-cm (5.2-6.9lb-in)

Torque sequence:



Heatsink Torquing Sequence

It is assumed that all four mounting screws are being torqued to a common surface.

Other thermal management schemes are at customer discretion as long as the maximum thermal rating of the specific module is not exceeded.

External Inrush Current Limit for APA100-101M

The difference between APA100-101M and APA100-101 is APA100-101M does not contain an internal inrush current limit circuit. Customer is requested to add an external inrush current limit circuit while using this model.

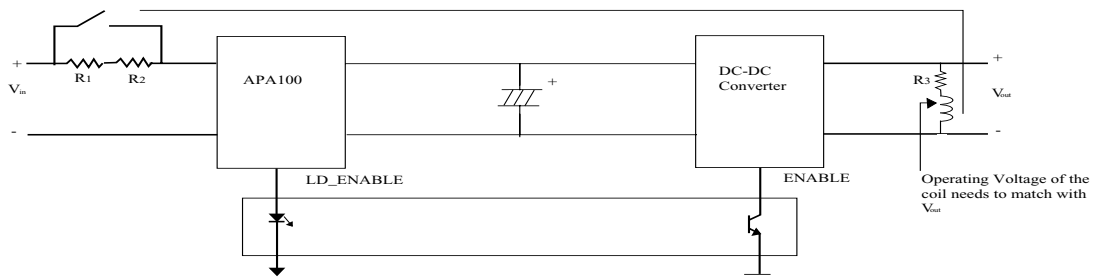
Below are two passive inrush current limit circuits for APA100-101M. Both use NTC thermistors to limit the inrush current during the startup period. The thermistors are bypassed by the relay switch during normal operating condition. For full load application, R1 and R2 can be Thinking's SCK0512, 5Ω. The relay can be one of the Song Chuan 793 series, depending on the supply for the coil voltage available in the customer system. If the system available supply voltage for the coil does not match with the relay, we can use a lower coil voltage relay and use R3 to balance the voltage for the coil, like a potential divider. If the supply voltage is same as the coil voltage, R3 can be eliminated.

If the system does not require full load operation, the customer can use a lower power rating thermistor and lower rating relay. If the power is low enough, the customer can consider using a single thermistor instead of two in series.

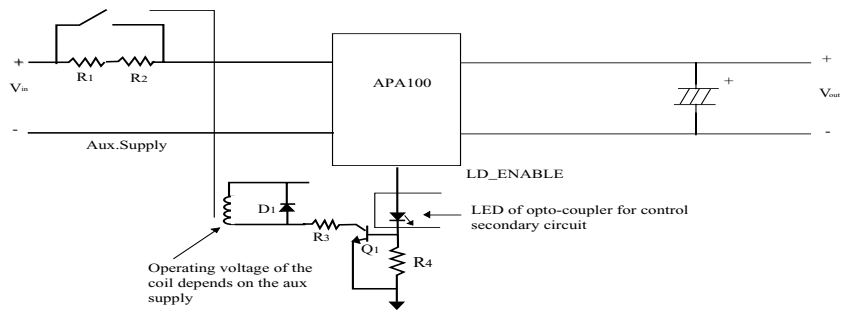
Since it is a thermistor design, the input power cycling speed cannot be too fast. It must provide enough time for the thermistor to cool down before the power is re-cycled. The cycling time is mainly dependent on the cooling speed of the thermistor.

Circuit 2 uses a primary supply for the relay. If there is no supply voltage on the primary side in the system design refer to Power Intergration component TY253 for a low power, physically small power supply design. Detail application information can be found in Power Integration WebSite, www.powerint.com

CIRCUIT(1): Using relay controlled from secondary side:



CIRCUIT(2):Using relay controlled by Auxiliary supply on primary side:



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