National Semiconductor

PRELIMINARY

MM58438 32-Bit LCD Display Driver

General Description

The MM58438 is a CMOS metal gate circuit which is capable of driving up to 32 LCD segments and is available in a 40-pin molded package. In addition, MM58438 dice is available for PCB module assembly systems. The circuit requires a minimum of interface between data source and display and can be cascaded where larger displays are required.

Features

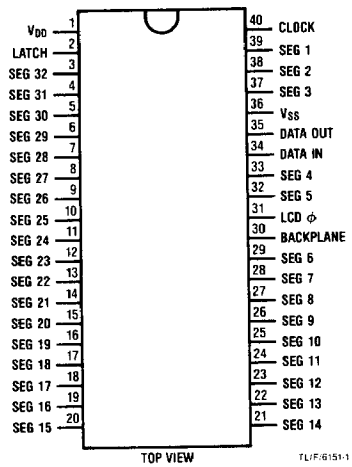
- Serial data input
- 32 segment outputs
- Cascaded operation capability
- Alphanumeric and bar graph capability
- TTL compatibility
- Non-multiplex display
- Compatible with HLCD 0438, HLCD 0438A
- Stable oscillator only requires one external component

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Digital clock, thermometer, counter, voltmeter displays
- Industrial control indicator
- Serial to parallel converter

Connection Diagram

Dual-In-Line Package



Order Number MM58438N
See NS Package N40A

Block Diagram

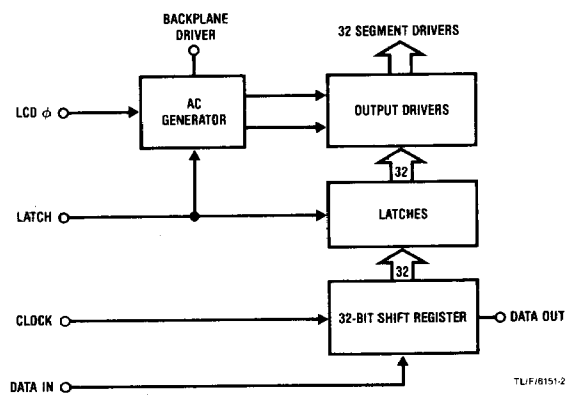


FIGURE 1

Absolute Maximum Ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
V_{DD} Supply Voltage	18V
Operating Temperature	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $V_{DD} = 3.0V$ to 15V, $T_A = -40°C$ to $+85°C$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{DD}		3.0		15	V
Supply Current I_{DD}	Oscillating or Driven Mode, $V_{DD} = 5V$			60	μA
Input High Level V_{IH}	$V_{DD} = 4.5V$ to 5.5V	2.4		V_{DD}	V
	$V_{DD} = 5.5V$ to 15V	0.5 V_{DD}		V_{DD}	V
Input Low Level V_{IL}	$V_{DD} = 4.5V$ to 5.5V	0		0.8	V
	$V_{DD} = 5.5V$ to 15V	0		0.1 V_{DD}	V
Input Current (Any Input)				±10	μA
Input Capacitance				10	pF
Output Current Levels					
Segments					
Sink I_{OL}	$V_{DD} = 4.5V$, $V_{OUT} = 0.2V$	20			μA
Source I_{OH}	$V_{DD} = 4.5V$, $V_{OUT} = V_{DD} - 0.2V$	20			μA
Backplane					
Sink I_{OL}	$V_{DD} = 4.5V$, $V_{OUT} = 0.2V$	320			μA
Source I_{OH}	$V_{DD} = 4.5V$, $V_{OUT} = V_{DD} - 0.2V$	320			μA
Output Offset Voltage	Segment Capacitance = 250 pF				
	Backplane Capacitance = 8750 pF			±50	mV
Data Output					
Sink	$V_{DD} = 4.5V$, $V_{OUT} = 0.5V$			−100	μA
Source	$V_{DD} = 4.5V$, $V_{OUT} = V_{DD} - 0.5V$	100			μA

AC Electrical Characteristics $V_{DD} = 3.0V$ to 15V, $T_A = -40°C$ to $+85°C$ unless otherwise specified *(Figure 2)*

Parameter	Conditions	Min	Typ	Max	Units
t1 Data Hold Time		0.1			μs
t2 Data Set-Up Time		0.1			μs
t3 Latch Pulse Width		1			μs
t4 Clock to Latch Time		0.1			μs
t_{pd} Data Out Delay				500	ns
Clock Frequency f		DC		500	kHz
Clock Period t (= 1/f)		2			μs
Backplane Frequency	$C_{EXT} = 47$ pF		100		Hz
Oscillator Stability	$V_{DD} = 5V$			±50	%
V_{DD} Rise Time	0V to 5V	5			ms

Functional Description

The connection diagram for the MM58438 is shown on the first page. The circuit is designed to drive LCD displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, SERIAL DATA, CLOCK and LATCH.

The MM58438 uses a latch mode of microprocessor data transfer whereby the signal LATCH acts as a latch to the input data *(Figure 2)*. Data is input to and output from the internal shift register on the negative clock edge (i.e., a logic '1' to logic '0' transition) while the LATCH pin is held low. The contents of the shift register are latched to the output latches and display drivers on the logic '0' to logic '1' transition of the LATCH pin when it is pulsed high.

The MM58438 can be cascaded when a larger display is required where it can be considered to be driven or oscillating.

In the oscillating mode, the BACKPLANE frequency is determined by the capacitor connected to the LCD ϕ pin. When two circuits are cascaded the second LCD ϕ input is driven by the first backplane output.

When the circuit is first powered on, an internal power on reset signal is generated which primes the mode detect logic and sets the BACKPLANE to a logical high level. If the circuit is in the oscillating mode the LCD ϕ pin is connected to a capacitor which is held low by a high impedance internal pull down transistor. If the circuit is in the driven mode the LCD ϕ pin is connected to the previous BACKPLANE output and is forced high by this low impedance output. When the first LATCH pulse goes to a logic '1' the level on the LCD ϕ pin is internally latched which indicates to the rest of the logic whether the circuit is driven or oscillating.

The oscillator on the oscillating device starts as soon as the LATCH pin goes to a logic '1'.

In the driven mode, the BACKPLANE frequency is in phase with the input frequency on the LCD ϕ.

To ensure the correct latching of this function, the LATCH input must be held at a logic '0' level for a minimum of 10 μs at power on.

Once the initial conditions on power up have been obeyed, the circuit can be used as serial to parallel converters with the polarity of the output data determined by the logic level on the LCD ϕ input. A logic '1' on the LCD ϕ input produces inverted data.

Timing Diagram

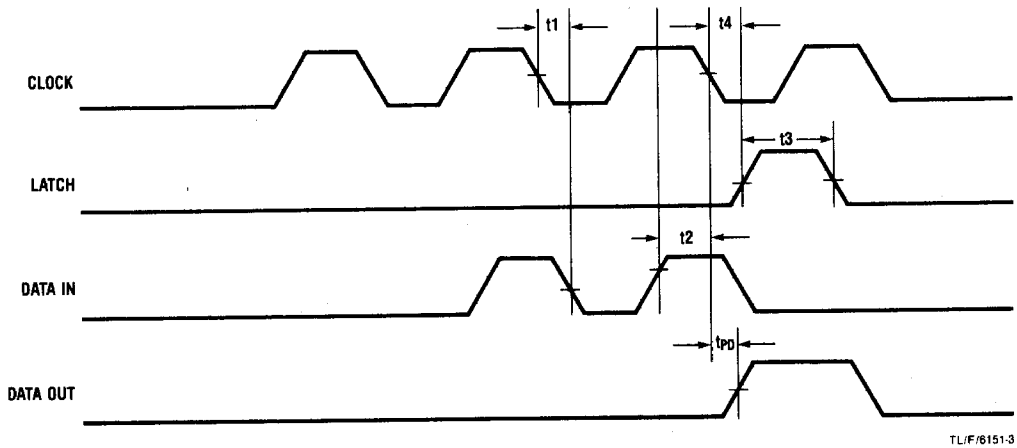


FIGURE 2

Typical Application

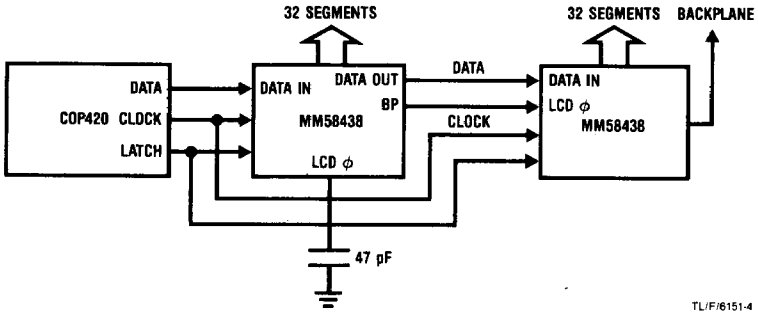


FIGURE 3. 64-Segment Display Cascading Two MM58438s